ABSTRACT OF THE DISCLOSURE

An auxiliary device for operating both M-DOC series flash memory and non-X86 system processor in synchronism is provided. The auxiliary device comprises a first logic circuit enabled by a first address line of the non-X86 system processor for changing output thereof from a first level to a second level, a delay circuit for delaying the second level output of the first logic circuit a predetermined period of time prior to clearing the first logic circuit for changing output thereof from a second level to a first level, and a second logic circuit for performing a logical operation on the output of the first logic circuit and a CS pin of the non-X86 system processor prior to coupling to a CS pin of the M-DOC series flash memory. The M-DOC series flash memory thus can be used as both a power on memory and a typical memory.